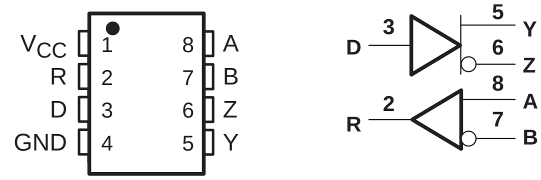
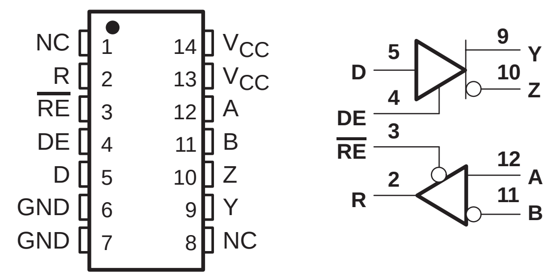
- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995 Standard**
- **Signaling Rates up to 155 Mbps**
- **Operates From a Single 3.3-V Supply**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV and a 100 Ω Load**
- **LVTTL Input Levels are 5 V Tolerant**
- **Driver is High Impedance When Disabled or With V_{CC} < 1.5 V**
- **Receiver has Open-Circuit Fail Safe**
- **Surface-Mount Packaging**
  - **D Package (SOIC)**
- **Characterized For Operation From 0°C to 70°C**

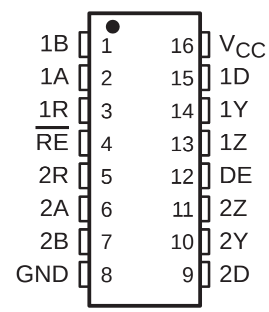
SN75LVDS179D (Marked as **DS179** or **7LS179**)
(TOP VIEW)

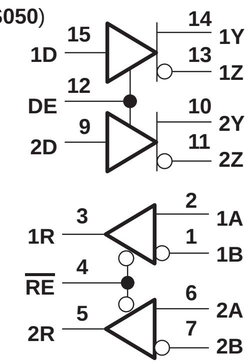


SN75LVDS180D (Marked as **7LVDS180**)
(TOP VIEW)

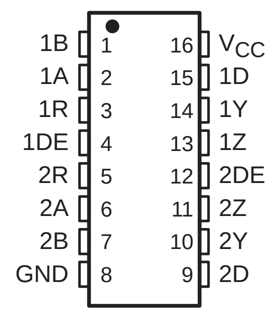


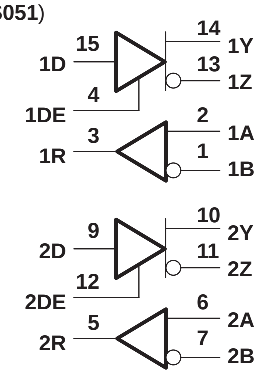
SN75LVDS050D (Marked as **75LVDS050**)
(TOP VIEW)





SN75LVDS051D (Marked as **75LVDS051**)
(TOP VIEW)





description

The SN75LVDS179, SN75LVDS180, SN75LVDS050, and SN75LVDS051 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 155 Mbps. The TIA/EIA-644 standard compliant electrical interface provides a minimum differential output voltage magnitude of 247 mV into a 100 Ω load and receipt of 100 mV signals with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics).

The SN75LVDS179, SN75LVDS180, SN75LVDS050, and SN75LVDS051 are characterized for operation from 0°C to 70°C.

Function Tables

SN75LVDS179 RECEIVER

INPUTS	OUTPUT
$V_{ID} = V_A – V_B$	R
$V_{ID} \geq 100$ mV	H
–100 MV < V_{ID} < 100 mV	?
$V_{ID} \leq –100$ mV	L
Open	H

H = high level, L = low level, ? = indeterminate

SN75LVDS179 DRIVER

INPUT	OUTPUTS	
D	Y	Z
L	L	H
H	H	L
Open	L	H

H = high level, L = low level

SN75LVDS180, SN75LVDS050, and SN75LVDS051 RECEIVER

INPUTS		OUTPUT
$V_{ID} = V_A – V_B$	$\overline{RE}$	R
$V_{ID} \geq 100$ mV	L	H
–100 MV < V_{ID} < 100 mV	L	?
$V_{ID} \leq –100$ mV	L	L
Open	L	H
X	H	Z

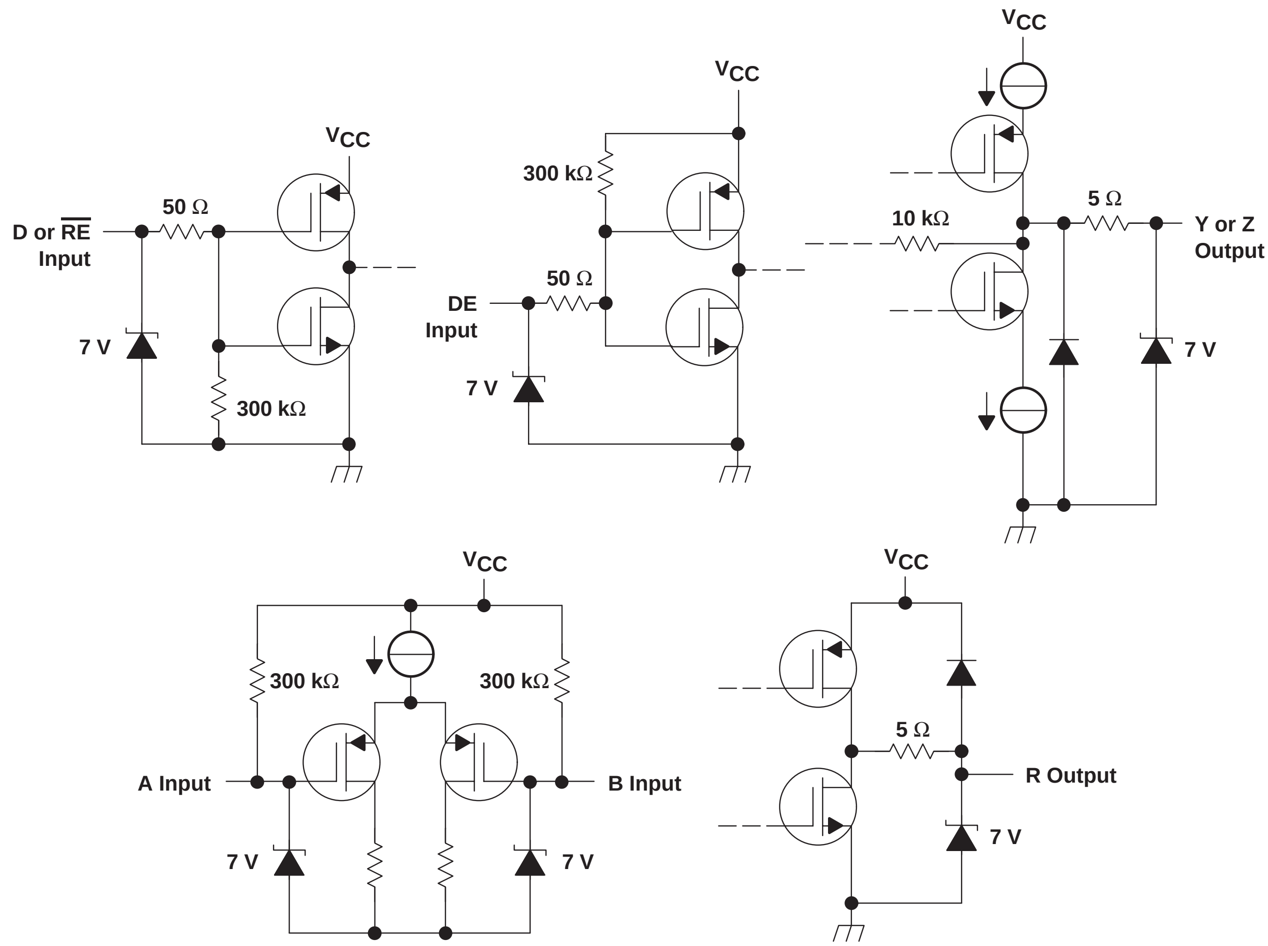
H = high level, L = low level, Z = high impedance, X = don’t care

SN75LVDS180, SN75LVDS050, and SN75LVDS051 DRIVER

INPUTS		OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

H = high level, L = low level, Z = high impedance, X = don’t care

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.5 V to 4 V
Voltage range (D, R, DE, $\overline{RE}$) . . . . –0.5 V to 6 V
Continuous power dissipation . . . . see dissipation rating table
Storage temperature range . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 250°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$†	$T_A = 70°C$ POWER RATING
D8	725 mW	5.8 mW/°C	464 mW
D14 or D16	950 mW	7.8 mW/°C	608 mW

† This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Magnitude of differential input voltage, $\lvert V_{ID} \rvert$	0.1		0.6	V
Common–mode input voltage, V_{IC} (see Figure 6)	$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	V
			V_{CC}–0.8	
Operating free–air temperature, T_A	0		70	°C

device electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}	Supply current	SN75LVDS179	No receiver load, driver R_L = 100 Ω		9	12	mA
		SN75LVDS180	Driver and receiver enabled, No receiver load, Driver R_L = 100 Ω		9	12	mA
			Driver enabled, receiver disabled, R_L = 100 Ω		5	7	
			Driver disabled, receiver enabled, No load		1.5	2	
			Disabled		0.5	1	
		SN75LVDS050	Drivers and receivers enabled, no receiver loads, Driver R_L = 100 Ω		12	20	mA
			Drivers enabled, receivers disabled, R_L = 100 Ω		10	16	
			Drivers disabled, receivers enabled, no loads		3	6	
			Disabled		0.5	1	
		SN75LVDS051	Drivers enabled, no receiver loads, driver R_L = 100 Ω		12	20	mA
			Drivers disabled, No loads		3	6	

† All typical values are at 25°C and with a 3.3-V supply.

driver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude		R_L = 100Ω, See Figure 1 and Figure 2	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states			–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 3	1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	mV
I_{IH}	High-level input current	DE	V_{IH} = 5 V		–0.5	–20	µA
		D			2	20	
I_{IL}	Low-level input current	DE	V_{IL} = 0.8 V		–0.5	–10	µA
		D			2	10	
I_{OS}	Short-circuit output current		V_{OY} or V_{OZ} = 0 V		3	10	mA
			V_{OD} = 0 V		3	10	
I_{OZ}	High-impedance output current		V_{OD} = 600 mV			±1	µA
			V_O = 0 V or V_{CC}			±1	
$I_{O(OFF)}$	Power-off output current		V_{CC} = 0 V, V_O = 3.6 V			±1	µA
C_{IN}	Input capacitance				3		pF

receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 5 and Table 1			100	mV
$V_{ITH–}$	Negative-going differential input voltage threshold		–100			
V_{OH}	High-level output voltage	I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current (A or B inputs)	V_I = 0	–2	–11	–20	μA
		V_I = 2.4 V	–1.2	–3		
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_{CC} = 0			±20	μA
I_{IH}	High-level input current (enables)	V_{IH} = 5 V			±10	μA
I_{IL}	Low-level input current (enables)	V_{IL} = 0.8 V			±10	μA
I_{OZ}	High-impedance output current	V_O = 0 or 5 V			±10	μA
C_I	Input capacitance			5		pF

† All typical values are at 25°C and with a 3.3-V supply.

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100Ω, C_L = 10 pF, See Figure 6			6	ns
t_{PHL}	Propagation delay time, high-to-low-level output				6	ns
t_r	Differential output signal rise time			0.8	1.2	ns
t_f	Differential output signal fall time			0.8	1.2	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} – t_{pLH}\|$)‡				0.6	ps
$t_{sk(o)}$	Channel-to-channel output skew§				0.6	ps
$t_{sk(pp)}$	Part-to-part skew¶				1	ps
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 7			25	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output				25	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output				25	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				25	ns

† All typical values are at 25°C and with a 3.3-V supply.
‡ $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output
§ $t_{sk(o)}$ is the magnitude of the time difference between the outputs of a single device with all of their inputs connected together.
¶ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 6		2.1	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output			2.1	6	ns
t_r	Output signal rise time			0.6	1.5	ns
t_f	Output signal fall time			0.7	1.5	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} – t_{pLH}\|$)‡				0.6	ns
$t_{sk(o)}$	Channel-to-channel output skew§				0.6	ns
$t_{sk(pp)}$	Part-to-part skew¶				1	ns
t_{PZH}	Propagation delay time, high-level-to-high-impedance output	See Figure 7			25	ns
t_{PZL}	Propagation delay time, low-level-to-low-impedance output				25	ns
t_{PHZ}	Propagation delay time, high-impedance-to-high-level output				25	ns
t_{PLZ}	Propagation delay time, low-impedance-to-high-level output				25	ns

† All typical values are at 25°C and with a 3.3-V supply.
‡ $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output
‡ $t_{sk(o)}$ is the magnitude of the time difference between the outputs of a single device with all of their inputs connected together.
‡ $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

driver

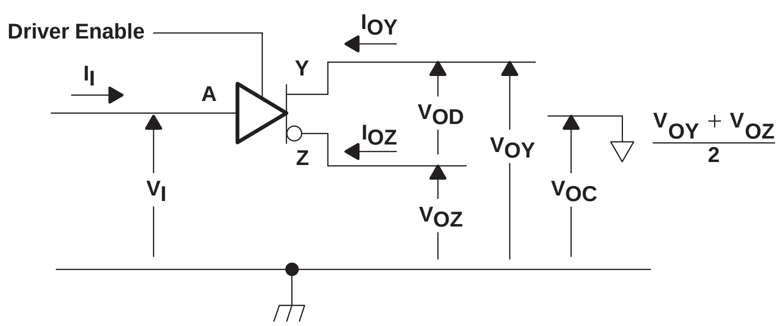
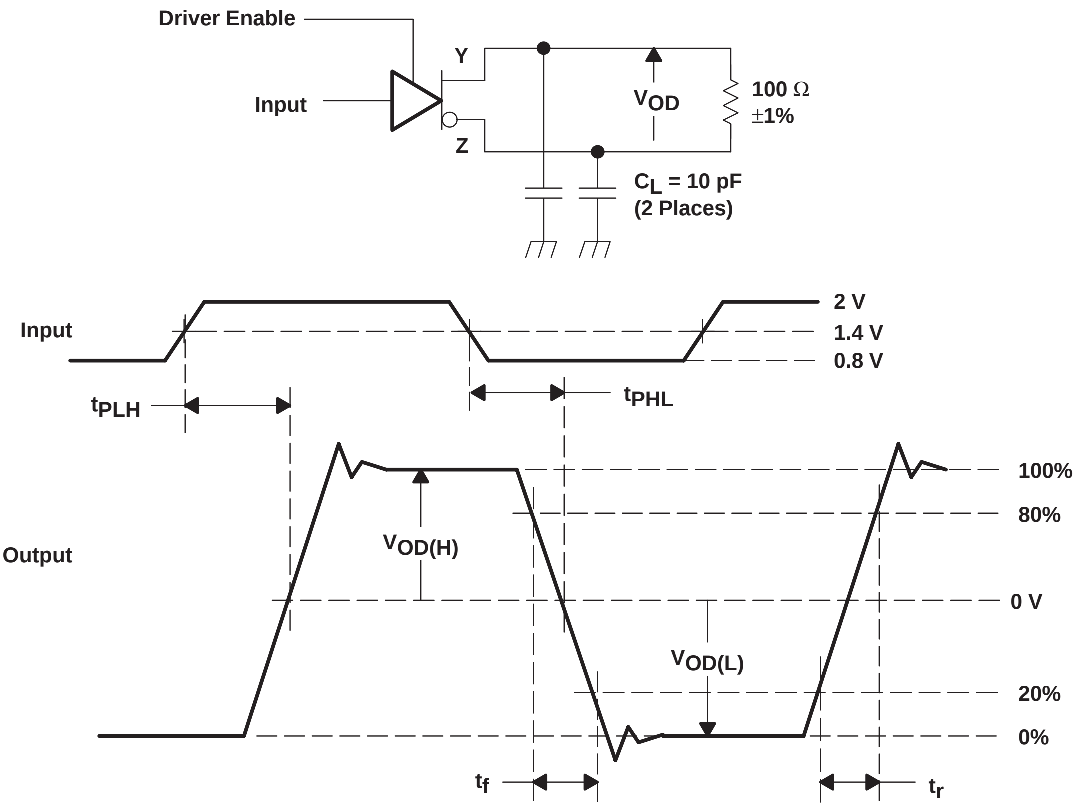


Figure 1. Driver Voltage and Current Definitions

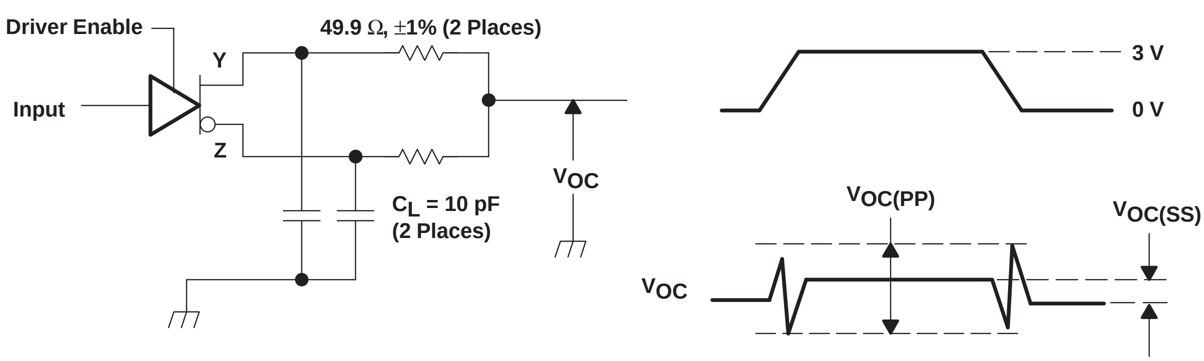
PARAMETER MEASUREMENT INFORMATION

driver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

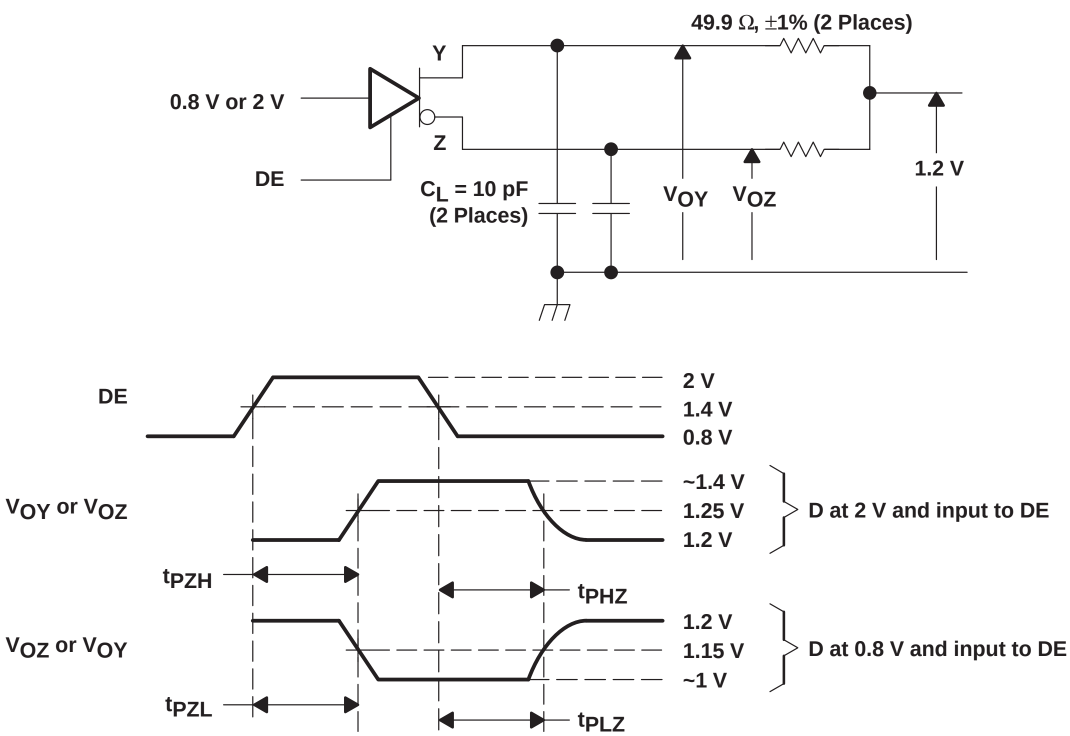


NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION

driver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Enable and Disable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION

receiver

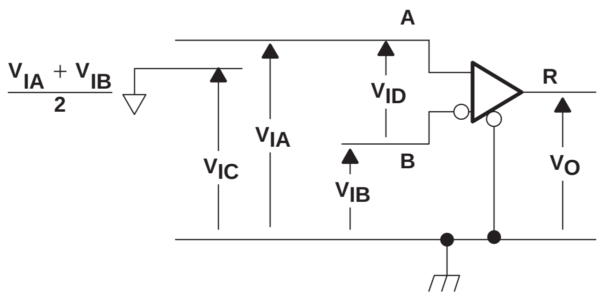


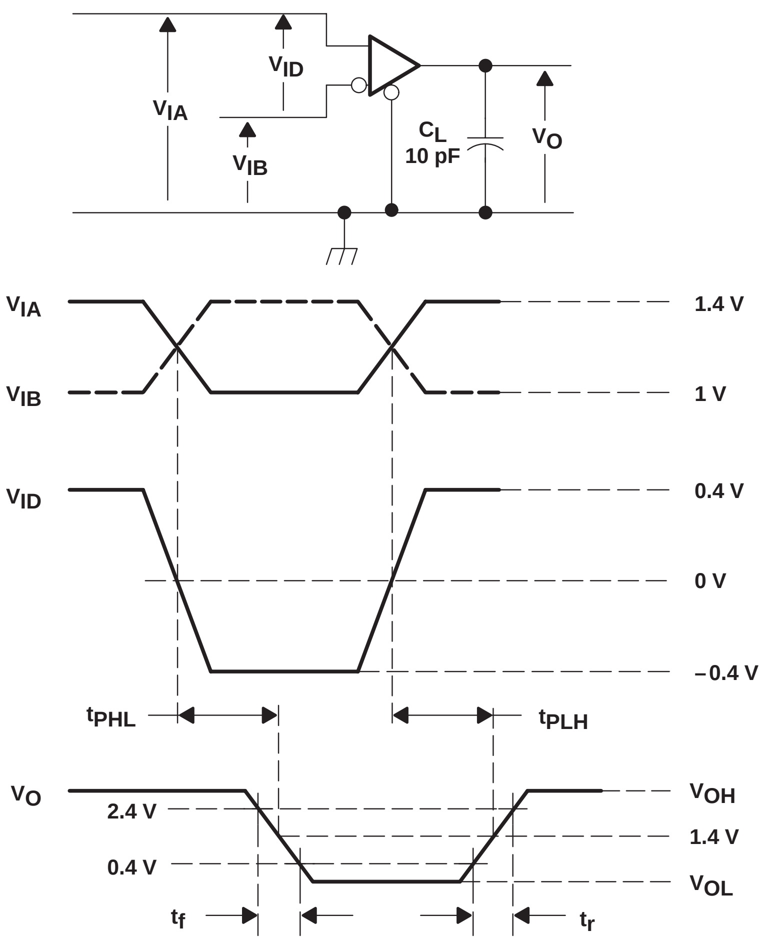
Figure 5. Receiver Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES (V)		RESULTING DIFFERENTIAL INPUT VOLTAGE (mV)	RESULTING COMMON-MODE INPUT VOLTAGE (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	–100	1.2
2.4	2.3	100	2.35
2.3	2.4	–100	2.35
0.1	0	100	0.05
0	0.1	–100	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3

PARAMETER MEASUREMENT INFORMATION

receiver (continued)

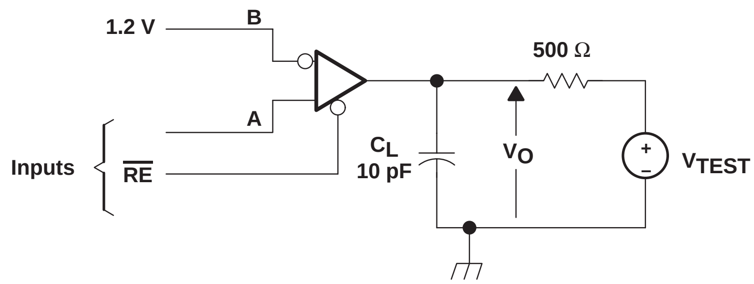


NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 6. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

receiver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

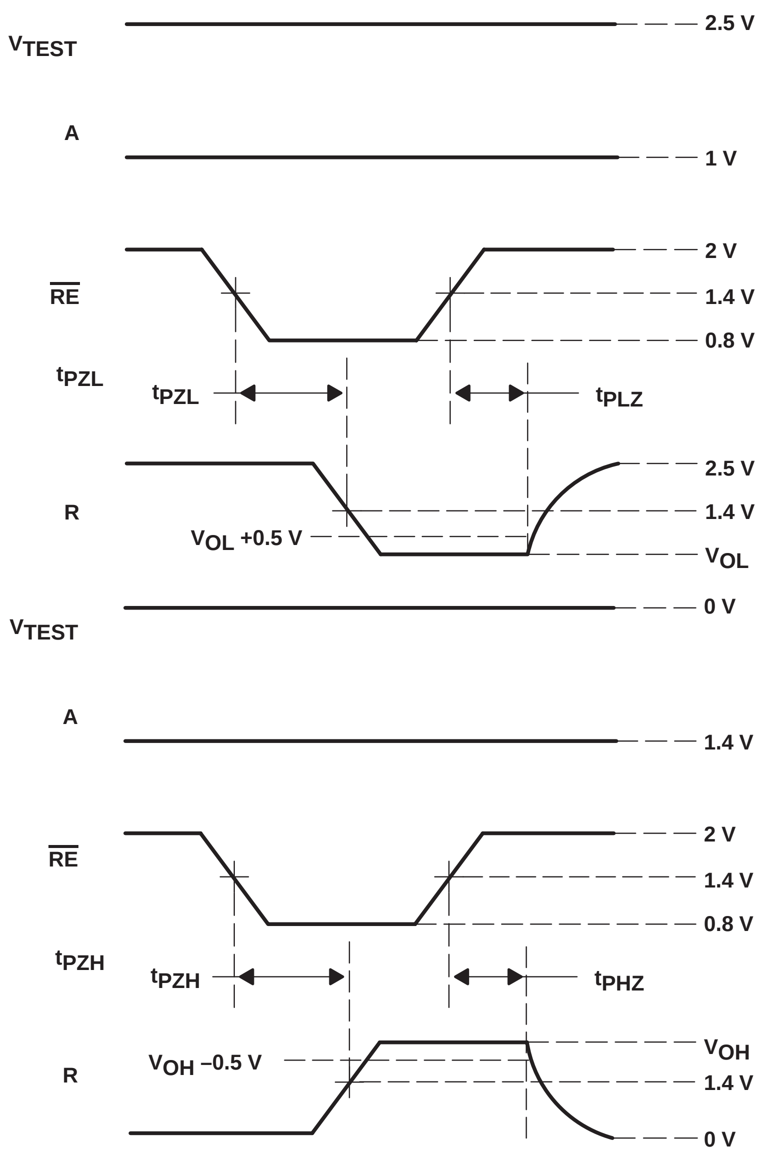


Figure 7. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

COMMON-MODE INPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

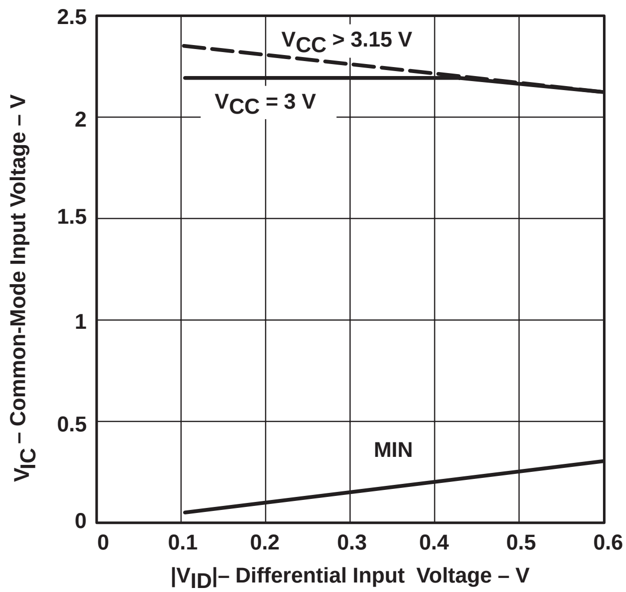


Figure 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

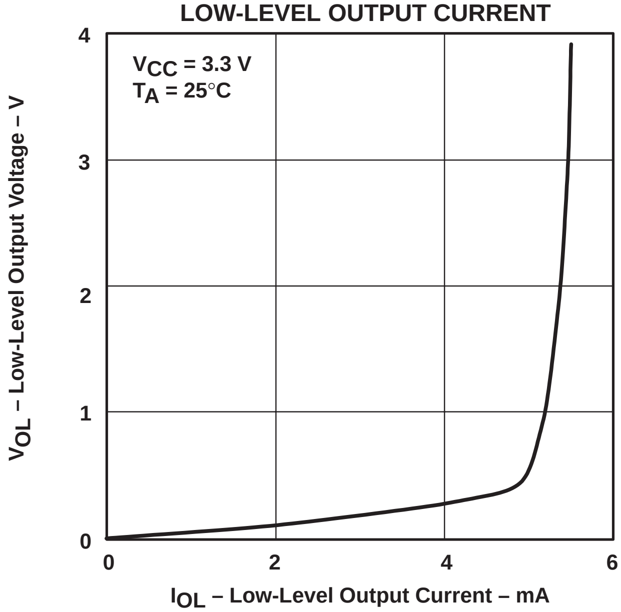


Figure 9

DRIVER HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

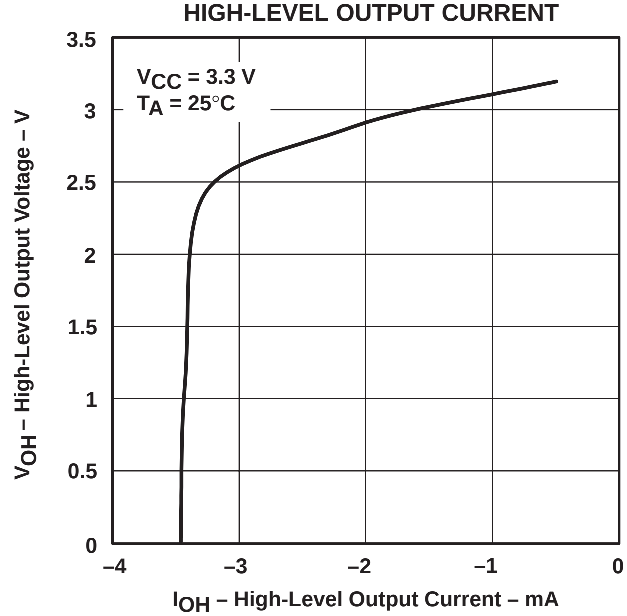


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

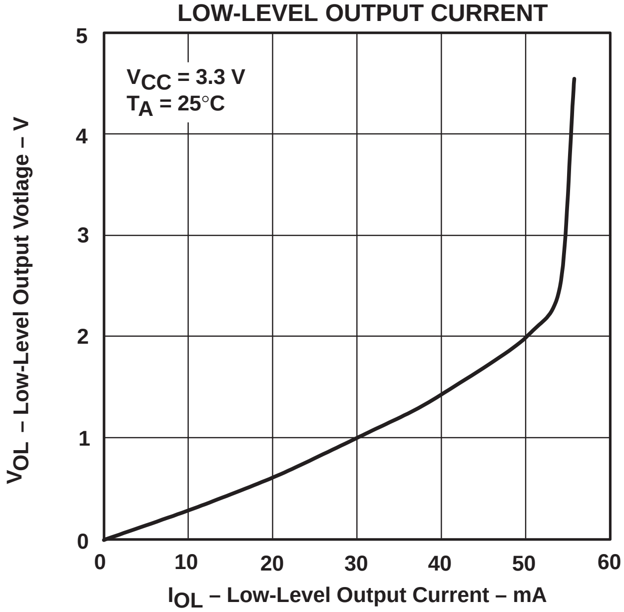


Figure 11

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

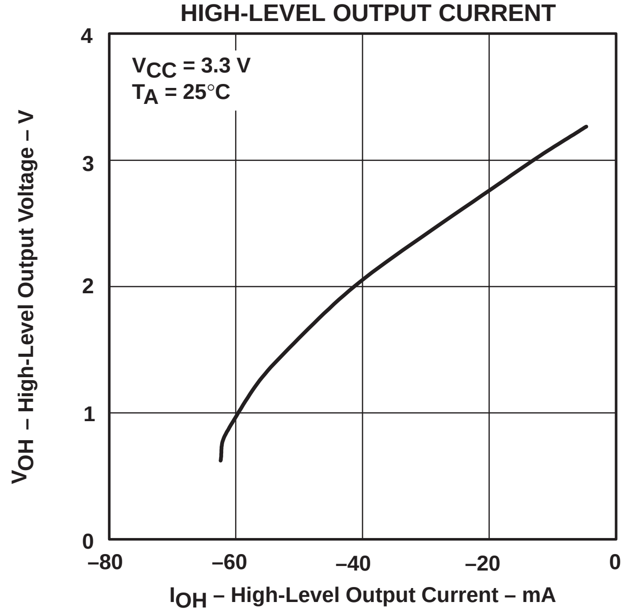


Figure 12

APPLICATION INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission. Ground differences are less than 1 V with a low common–mode output and balanced interface for very low noise emissions. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/Receivers maintain ECL speeds without the power and dual supply requirements.

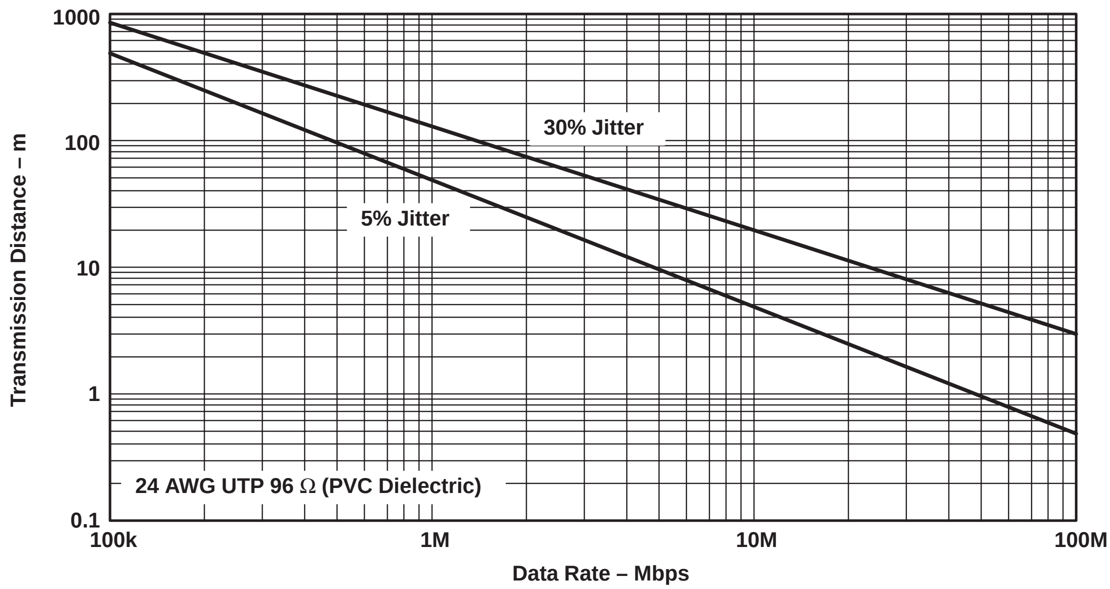


Figure 13. Data Transmission Distance Versus Rate

APPLICATION INFORMATION

fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 14. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

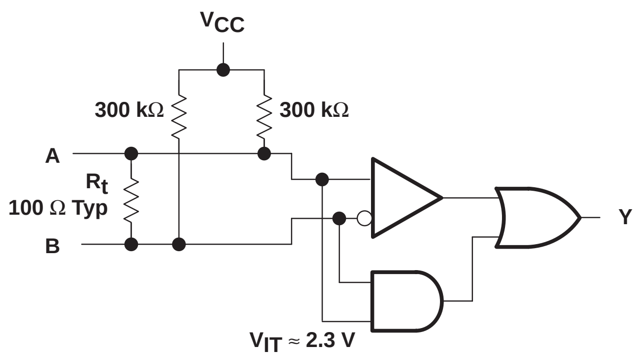


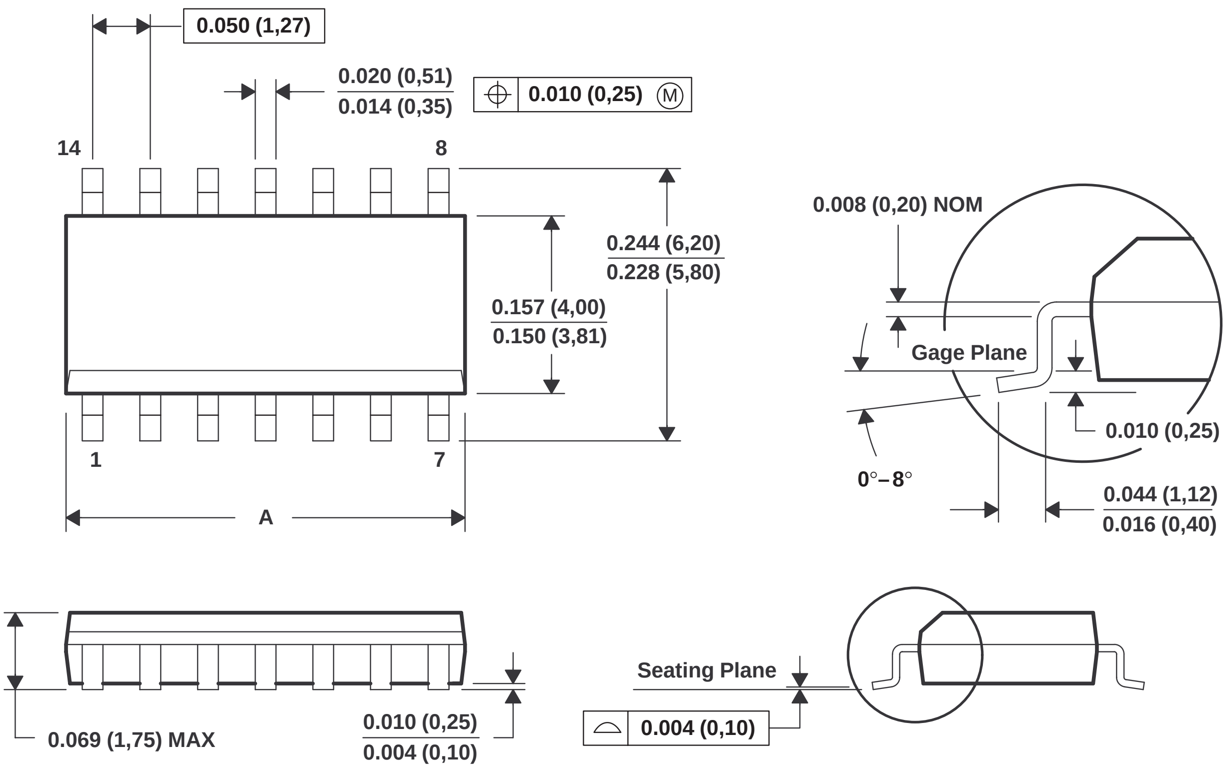
Figure 14. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75LVDS051D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS051DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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